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10/614,067	07/03/2003	Glen J. Leedy	ELM-2 DIV . 6	8117

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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/614,067	LEEDY, GLEN J.	
	Examin r	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *88-154,156-164,166 and 167* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *146-154,156-164,166 and 167* is/are allowed.

6)☒ Claim(s) *88-124,126,127 and 129* is/are rejected.

7)☒ Claim(s) *125,128 and 130-145* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the RCE on 19 April 2006. Claims 88-154, 156-164, 166 and 167 are pending; claims 155 and 165 have been cancelled.

The indicated allowability of claims 88-145, 149 and 159 is withdrawn in view of the newly discovered reference(s) drawn to the definition of monolithic. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 88-124, 126, 127 and 129 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faris (5,786,629) in view of Wojnarowski (5,324,687).

Referring to claims 88, 97, 146 and 156, Faris discloses an integrated circuit structure including a plurality of semiconductor dice (2), each die having an integrated circuit (6) formed thereon, the dice (2) being stacked in layers, wherein at least one of the plurality of dice is substantially flexible; and between adjacent dice, a bonding layer (17) bonding together the adjacent dice, the bonding layer bonding first and second substantially planar adjacent surfaces of the adjacent dice (Fig. 4; col. 6, lines 12-27; col. 7, lines 1-12; col. 8, lines 1-7). Although, Faris does not specifically disclose the

semiconductor dice as monolithic substrate, they are inherently the same. Webster's Dictionary defines monolithic as a single uniform piece.

Faris does not disclose at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice.

Wojnarowski discloses circuitry comprising a plurality of substrates (10, 30) having integrated circuits (12, 14) formed thereon (Fig. 3; col. 5, lines 25- 53), wherein at least one of the plurality of substrates is a substantially flexible substrate (Fig. 7; col. 8, lines 10-38); and between adjacent substrates (10, 30), a bonding layer (28) bonding together the adjacent substrates (10, 30), the bonding layer (28) being formed by bonding first and second substantially planar surfaces having a bond-forming material throughout a majority of the surface area thereof, wherein at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice (Fig. 3; col. 5, lines 36-66).

Since Faris and Wojnarowski are both from the same field of endeavor, an integrated circuit device, the purpose disclosed by Wojnarowski would have been recognized in the pertinent art of Faris. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Faris by at least one or more portions of the bonding layer being located other than at the edges of the adjacent dice as taught by Wojnarowski to product flexible circuit packages or modules (col. 1, lines 62-65).

Referring to claims 89-90 and 95-96, Wojnarowski discloses vertical interconnects having vertical interconnect segments formed of a first metal contact on a

first substrate bonded to a second aligned metal contact on a second adjacent substrate, wherein the plurality of aligned vertical interconnect segments are joined to form a vertical interconnect between non-adjacent substrates. Forming the vertical interconnects formed between the adjacent bonded substrates to interconnect the integrated circuits in subsequent processing steps. (Fig. 8, col. 9, line 60 thru col. 10, line 61).

Referring to claims 91-92, Wojnarowski discloses at least one of said substrates is a substantially rigid substrate having a first thickness, wherein a plurality of substrates have a reduced thickness substantially less than said first thickness (Fig. 1 & 2: col. 5, lines 25-53).

Referring to claims 93 and 94, Wojnarowski discloses the claimed invention except for ratio of the first thickness of the substrate to the second thickness as approximately 10:1. It would have been obvious to one having ordinary skill in the art at the time invention was made to have the ratio of the first thickness of the substrate to the second thickness as approximately 10:1, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Referring to claims 98-100, Wojnarowski discloses the second substrate is a thinned polycrystalline semiconductor substrate having active circuitry (12) and passive circuitry (14) formed thereon (Fig. 3; col. 5, lines 36-66).

Referring to claim 101, Wojnarowski discloses a stacked integrated circuit comprising a plurality of integrated circuit substrates (10, 30) having formed on corresponding surfaces thereof complementary patterns of a material (28) bondable using thermal diffusion bonding (Fig. 3; col. 5, lines 36-66), wherein at least one of the plurality of substrates is a substantially flexible integrated circuit substrate (Fig. 7; col. 8, lines 10-38); and a thermal diffusion bonded region between the complementary patterns (col. 5, lines 36-66).

Referring to claim 102, Wojnarowski discloses at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one integrated circuit substrates that has memory circuitry formed thereon is used instead of date from a defective memory location on the at least one integrated circuit substrate that has memory circuitry formed thereon (col. 8, lines 50-68).

Referring to claim 103, Wojnarowski discloses at least one integrated circuit substrate of the plurality of integrated circuit substrates has memory circuitry formed thereon and at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon, wherein the at least one circuitry formed thereon, integrated circuit substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one integrated circuit has memory circuitry formed thereon (col. 4,lines 13-38; col. 10, lines 13-27).

Referring to claim 104, Wojnarowski discloses information processing is performed on data routed between circuitry of at least two of the plurality of integrated circuit substrates (col. 10, lines 13-50).

Referring to claim 105, Wojnarowski discloses at least one integrated circuit substrate of the plurality of integrated circuit substrates has reconfiguration circuitry (col. 5, lines 36-66).

Referring to claim 106, Wojnarowski discloses at least one integrated circuit substrate of the plurality of integrated circuit substrates has logic circuitry formed thereon for performing at least one function from the group consisting of: virtual memory management, ECC, indirect addressing, content addressing, data compression, data decompression, graphics acceleration, audio encoding, audio decoding, video encoding, video decoding, voice recognition, handwriting recognition, power management and database processing (col. 1, line 33 thru col. 2, line 27).

Referring to claim 107, Wojnarowski discloses a memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores a data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines; circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and a controller that determines if on of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective (col. 8, lines 50-68; col. 10, lines 13-49).

Referring to claim 108, Wojnarowski discloses at least one controller substrate having logic circuitry formed thereon; at least one memory substrate having memory circuitry formed thereon; a plurality of data lines and a plurality of gate lines on each memory substrate; an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines; a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which of the plurality of gate lines is selected for each programmed address assignment; and controller substrate logic that determines if one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines (col. 8, lines 50-68; col. 10, lines 13-39).

Referring to claim 109, Wojnarowski discloses the controller substrate logic tests the array of memory cells periodically to determine if one of said memory cells is defective; and removers references in the address assignments to gate lines that cause detected defective memory cells to couple data values to the plurality of data lines (col. 8, lines 50-68).

Referring to claim 110, Wojnarowski discloses programmable logic to prevent the use of data values from the plurality of data lines when gate lines cause detected

defective memory cells to couple data values to the plurality of data lines (col. 8,lines 50-68).

Referring to claim 111, Wojnarowski discloses the array of memory cells are arranged within physical space in a physical order and are arranged within an address space in a logical order, wherein the physical order of at least one memory cell is different than the logical order of the at least one memory cell (col. 10, lines 13-49).

Referring to claim 112, Wojnarowski discloses the logic circuitry of the at least one controller substrate is tested by an external means; and the array of memory cells of the at least one memory substrate are tested by the logic circuitry of the at least one controller substrate, wherein the testing achieves a functional testing of a substantial portion of the array of memory cells (col. 8, lines 50-68).

Referring to claim 113, Wojnarowski discloses the logic circuitry of the at least one controller substrate performs functional testing of a substantial portion of the array of memory cells (col. 8, lines 50-68).

Referring to claim 114, Wojnarowski discloses the controller substrate logic is further configured to prevent the use of at least one defective gate line; and replace references to memory cells addressed using the defective gate line with references to spare memory cells addressed using a spare gate line (col. 8, lines 50-68).

Referring to claim 115, Wojnarowski discloses the controller substrate logic is further configured to prevent the use of at least one defective gate line (col. 8, lines 50-68).

Referring to claim 116, Wojnarowski discloses the logic circuitry of the at least one controller substrate performs all functional testing of the array of memory cells of the at least one memory substrate (col. 8, lines 50-68).

Referring to claim 117, Wojnarowski discloses at least one of the plurality of integrated circuit substrates is a thinned substantially flexible substrate (col. 8, lines 10-38).

Referring to claim 118, Wojnarowski discloses the active circuitry is formed with a low stress dielectric (Fig. 1; col. 4, lines 12-38).

Referring to claim 120, Wojnarowski discloses at least one of the plurality of integrated circuit substrates is formed with a low stress dielectric (Fig. 1; col. 4, lines 12-38).

Referring to claim 122, Wojnarowski discloses at least one of the first substrate and the second substrate is a thinned substantially flexible substrate (Fig. 7; col. 8, lines 10-38).

Referring to claim 123, Wojnarowski discloses the active circuitry is formed with a low stress dielectric (Fig. 1; col. 4, lines 12-38).

Referring to claims 119, 121 and 124, Wojnarowski does not disclose the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less. It would have been obvious to one having ordinary skill in the art at the time invention was made to have the low stress dielectric is at least one of a silicon dioxide dielectric and caused to have stress of about $5x10^8$ dynes/cm^2 or less disclosed in the claimed invention, since it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Referring to claims 126, Faris discloses wherein at least one substrate of the first and second substrates has memory circuitry formed thereon and at least one of the first and second substrates has logic circuitry formed thereon, wherein the at least one substrate that has logic circuitry formed thereon performs programmable gate line address assignment with respect to the at least one substrate that has memory circuitry formed thereon (col. 3, lines 42-62).

Referring to claim 127, Faris discloses wherein information processing is performed on data routed between the first and second substrates (col. 3, lines 55-58).

Referring to claim 129, Faris discloses wherein at least one substrate of the first and second substrates has logic circuitry formed thereon for performing at least one function of data compression, data decompression, audio encoding, audio decoding, video encoding and database processing (col. 3, lines 48-55).

Allowable Subject Matter

Claims 146-154, 156-164, 166 and 167 are allowed.

Claims 125, 128 and 130-145 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: prior art does not anticipate, teach, or suggest referring to claim 125 wherein at least one substrate of the first and second substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the least one substrate that has memory circuitry formed thereon.

Referring to claims 128, 146 and 156, prior art does not anticipate, teach, or suggest wherein at least one substrate of the first and second substrates has reconfiguration circuitry.

Referring to claim 130, prior art does not anticipate, teach, or suggest the memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines; circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and controller that determines one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

Referring to claims 131-139, prior art does not anticipate, teach, or suggest at least one controller substrate having logic circuitry formed thereon; at least one memory substrate having memory circuitry formed thereon; a plurality of data lines and a plurality of gate lines on each memory substrate; an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines; a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which the plurality of gate lines is selected for each programmed address assignment; and controller substrate logic that determines one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

Referring to claims 140-142, 149 and 159, prior art does not anticipate, teach, or suggest the stress of the low stress dielectric is tensile.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
6 June 2006

Zandra V. Smith
Supervisory Patent Examiner
8 June 2006